Amendments to the Claims

1. (currently amended) A memory cell, comprising:

a semiconductor substrate having at least one trench formed in a surface thereof;

a recessed channel region of a first conductivity type semiconductor formed in the semiconductor substrate at the bottom of each trench;

a source region and a drain region both of a second conductivity type semiconductor formed in the semiconductor substrate on opposing sides of each trench, said source and drain region extending to substantially the bottom of said trench;

a gate dielectric layer formed on the semiconductor substrate, said gate dielectric layer being formed along the bottom and sidewalls of the trench; and

a control gate layer formed over the gate dielectric layer above the recessed channel region.

2. (canceled)

3. (original) The memory cell of claim 1, wherein the thickness of the gate dielectric layer between the top surface of the gate dielectric layer and the bottom surface of the gate dielectric layer is between 100 and 300 angstroms in thickness.

4. (original) The memory cell of claim 1, wherein the semiconductor substrate is a silicon-on-insulator (SOI) semiconductor substrate.

5. (original) The memory cell of claim 1, wherein the semiconductor substrate is a bulk silicon semiconductor substrate.

6. (original) The memory cell of claim 1, wherein the memory cell is a silicon-oxide-nitride-oxide-silicon (SONOS) device.

7. (original) The memory cell of claim 6, wherein the gate dielectric layer is an oxide-nitride-oxide (ONO) layer.

8. (original) The memory cell of claim 7, wherein the ONO layer is formed in the trench region so as to insulate the nitride layer from a floor region and a plurality of sidewall regions within the trench region.

9. (original) The memory cell of claim 1, wherein the gate dielectric layer extends above the source region and the drain region.

10. (original) The memory cell of claim 1, wherein the gate dielectric layer is comprised of a standard-K dielectric material.

11. (original) The memory cell of claim 1, wherein the gate dielectric layer is comprised of a high-K dielectric material.

12. (original) The memory cell of claim 11, wherein the high-K material is Al_2O_3.

13. (original) The memory cell of claim 1, further comprising:

a floating gate layer formed in the trench region and over the gate dielectric layer, said floating gate layer positioned between the source region and the drain region; and

an intergate dielectric layer disposed between the floating gate layer and the control gate layer.

14. (original) The memory cell of claim 13, wherein the thickness of the gate dielectric layer between the top surface of the gate dielectric layer and the bottom surface of the gate dielectric layer is between 50 and 150 angstroms in thickness.

15. (original) The memory cell of claim 13, wherein the semiconductor substrate is a silicon-on-insulator (SOI) semiconductor substrate.

16. (original) The memory cell of claim 13, wherein the semiconductor substrate is a bulk silicon semiconductor substrate.

17. (original) The memory cell of claim 13, wherein the intergate dielectric layer is an oxide-nitride-oxide (ONO) layer.

18. (currently amended) A method of fabricating a memory cell, comprising the steps of:

forming at least one trench in a surface of a semiconductor substrate;

forming a recessed channel region of a first conductivity type semiconductor in the semiconductor substrate at the bottom of each trench;

forming a source region and a drain region both of a second conductivity type semiconductor in the semiconductor substrate on opposing sides of each trench, said source and drain region extending substantially to the bottom of said trench;

forming a gate dielectric layer on the semiconductor substrate, said gate dielectric layer being formed along the bottom and sidewalls of the trench; and

forming a control gate layer over the gate dielectric layer above the recessed channel region.

19. (canceled)

20. (original) The method of claim 18, further comprising the step of:

forming the gate dielectric layer between the top surface of the gate dielectric layer and the bottom surface of the gate dielectric layer between 100 and 300 angstroms in thickness.

21. (original) The method of claim 18, further comprising the step of:

using a silicon-on-insulator (SOI) semiconductor substrate as the semiconductor substrate.

22. (original) The method of claim 18, further comprising the step of:

using a bulk silicon semiconductor substrate as the semiconductor substrate.

23. (original) The method of claim 18, further comprising the step of:
using an oxide-nitride-oxide (ONO) layer to form the gate dielectric layer.

24. (original) The method of claim 23, further comprising the step of:
forming the ONO layer in the trench region so as to insulate the nitride layer from a floor region and a plurality of sidewall regions within the trench region.

25. (original) The method of claim 18, further comprising the step of:
extending the gate dielectric layer above the source region and the drain region.

26. (original) The method of claim 18, further comprising the step of:
using a standard-K dielectric material to form the gate dielectric layer.

27. (original) The method of claim 18, further comprising the step of:
using a high-K dielectric material to form the gate dielectric layer.

28. (original) The method of claim 27, wherein the step of using a high-K material to form the gate dielectric layer includes using Al_2O_3.

29. (original) The method of claim 18, further comprising the steps of:
forming a floating gate layer in the trench region of the gate dielectric layer, the floating gate layer positioned between the source region and the drain region; and
forming an intergate dielectric layer between the floating gate layer and the control gate layer.

30. (original) The method of claim 29, further comprising the step of:

forming the gate dielectric layer between the top surface of the gate dielectric layer and the bottom surface of the gate dielectric layer between 50 and 150 angstroms in thickness.

31. (original) The method of claim 29, further comprising the step of:

using a silicon-on-insulator (SOI) semiconductor substrate as the semiconductor substrate.

32. (original) The method of claim 29, further comprising the step of:

using a bulk silicon semiconductor substrate as the semiconductor substrate.

33. (original) The method of claim 29, further comprising the step of:

using an oxide-nitride-oxide (ONO) layer to form the intergate dielectric layer.